REMARKS

Claims 1-14 are pending in the application and have been examined. Claims 1, 2 and 4 have been rejected and claims 3 and 5-12 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to include the limitations of the base claim and any intervening claims. Claims 13 and 14 have been allowed.

I. Claim Rejections under 35 U.S.C. §103(a)

Claims 1 and 2 were rejected under 35 U.S.C. §103(a) as being unpatentable over Mizokami et al. (U.S. Patent No. 5,523,991). In addition, claim 4 was rejected under §103(a) as unpatentable over the above reference in view of Kato et al. (U.S. Patent No. 4,544,962). In view of the following comments, Applicants respectfully traverse the rejections of these claims.

Summary of the Present Invention

The present invention relates to a method of transmitting digital data in which the data is retained in sectors each comprised of plurality of sync frames and sequentially transmitting the digital data. An object of the invention is to provide a transmitting method whereby digital data can be reproduced at a high precision even during high-density recording or data transmission, such as in a Digital Video Disk (DVD). The reason behind this object is to cure problems present in the prior art. Specifically, in a CD player, a sync signal is extracted by

detecting a repetitive pattern of 11T (e.g., 11T - 11T) from an Eight to Fourteen (EFM) modulated signal read out from the CD. However, when reading information from a DVD, the information is largely influenced by an inter-symbol interference. The repetitive pattern of 11T used as a sync signal, is changed to a pattern such as 11T - 10T, for example, due to edge shifting of the sync signal due to the inter-symbol interference which leads to erroneous sync signal detection.

To cure this problem, the method of the present invention includes, *inter alia*, constructing a sync pattern within a 32 bit sync signal at bits 11 through 32 from data received from a 8-16 (eight to sixteen bit) modulator with an arrangement of a pattern 14T as the nucleus being larger than a maximum interval 11T in the 8-16 modulation signal by 3T. Also, an addition pattern of a fixed length 4T and another addition pattern of 4T or more are arranged after and before the pattern of 14T, respectively. The 14T pattern denotes a shortest length which can be set when considering edge-shift due to inter-symbol interference. Thus, even when the 11T pattern in the 8-16 modulation signal is edge-shifted due to an influence by an inter-symbol interference and is changed to a pattern of 12T, for example, the sync pattern can be distinguished since the pattern of 14T is larger than the maximum interval 11T by 3T in the 8-16 modulation signal. Further, by arranging the addition bit patterns after and before the 14T pattern, an interval that is larger than the shortest bits of 3T by at least 1T is provided, thereby reducing the influence of the inter-symbol interference with neighboring bits.

An additional feature of the present invention involves adding a specific code to bits 4 to 10 of the 32 bit sync signal. This specific code is used to indicate the position of the sync signal within the sector. In addition, the specific code is used by a CPU controlling a synthesizing means 30 generating the data transmission signal to select sync patterns which are optimum for DC suppression.

Summary of Mizokami et al.

The invention of Mizokami et al. relates to a data recording/reproducing device which attains an accurate re-synchronization in recording/reproducing data by an edge recording method. When recording data on a recording medium, a synchronization (sync) signal is inserted at regular intervals in the data converted into run-length limited code to form status transition patterns such as pits in a data recording area of the recording medium. On the other hand, when reproducing the data recorded in this manner, the sync signal detected from the recording medium is separated into a signal (leading edge data) corresponding to the leading edge of each status transition pattern and a signal (trailing edge data) corresponding to the trailing edge of each status transition pattern. Using these two sync signals (termed "re-sync signals"), Mizokami et al. re-composes the leading edge data and the trailing edge data into a reproduced data having correction of a deviation in the relative positional relation between the two types of data.

In particular, Figure 2 of Mizokami et al. illustrates a 2-7 code rule in which the codes of only two successive "0"s of the minimum run length follows immediately after the code of seven successive "0"s of the maximum run-length. The number of successive "0"s between "1" and "1" is two at minimum and seven at maximum. Figure 3A illustrates the sync signal 24 according the above conversion rule. When this sync signal is recorded onto an optical disk, for example, a pit pattern 25 is created. When reading the signal, a signal separation circuit (13 as shown in Figure 1) reads out the leading edge data 26 and the trailing edge data 27. This data is then utilized by clock synchronization circuits (14 and 15) for creating reproduction clocks which produce leading edge data and trailing edge data in synchronization with these clocks. Pattern detecting circuits 16 and 17 detect sync signals for re-synchronization for the leading and trailing edge data, respectively. A reproduced data composing circuit 18 is then used for composing the leading edge data and trailing edge data which also corrects changes in the relative positional relationship between the leading edge data and trailing edge data by using first and second RESYNC detection signals.

Summary of Kato et al.

Kato et al. is drawn to a method and apparatus for processing binary data prior to magnetic recording to the data. The data is divided into 4-bit data segments which are converted to 8-bit codes according to a predetermined encoding transfer function. Included in the method is a step of generating a frame synchronization code and interleaving it with 8-bit codes to form

a frame of binary digits. These 8-bit codes are supplied in parallel to a shift register 26 which, in turn, is read out in a stream of 32 bits to form a frame sync code 52 as illustrated in Figure 2. In addition, 32 bits of cyclic redundant check code (CRCC) 56 is also read out into the stream of data.

Analysis of the Rejection under §103

In rejecting claim 1, the Examiner asserts that Mizokami et al. discloses all the elements of the claimed method except for the run length of the bit pattern being longer than the maximum run length by 3T and the run length of the addition bits being longer than minimum run length. In order to make up for the shortcomings of Mizokami et al., the Examiner asserts that it would have been obvious to one of ordinary skill in the art to modify the teachings of the reference to use run lengths "of the patterns in the sync pattern for comparing the lengths of the patterns because it permits [the] system to readily recapture a sync frame code that occurs subsequent to the occurrence of a frame sync error to thereby minimize the out of sync period to at most one frame interval."

Applicants assert that the cited reference does not include all the limitations of the claimed invention and that the Examiner has not properly provided evidence or teaching in the reference or knowledge in the art that it would have been obvious to modify Mizokami et al. to arrive at the present claimed method. Specifically, the present claimed method includes "a sync pattern comprised of a bit pattern of a run length which is longer than said maximum run length

by 3T and addition bit patterns which are arranged before and after said bit pattern and each of which has a run length that is longer than said minimum run length." As accurately recognized by the Examiner, these limitations are not explicitly disclosed by Mizokami et al. However, these limitations are further not inherent or suggested by Mizokami et al. Thus, the reference itself does not teach or suggest the present claimed invention.

Notwithstanding the foregoing, the Examiner nonetheless asserts that it would have been obvious to modify the reference to include the above recited limitations based upon what appears to be an asserted motivation gleaned from knowledge commonly known in the art. However, neither evidence nor explanation of how modifying the reference to "use . . . run lengths of the patterns in the sync pattern for comparing the lengths of patterns . . . permits the system to readily recapture a sync frame code that occurs subsequent to the occurrence of a frame sync error to thereby minimize the out of sync period to at most one frame interval" has been provided to support the rejection. To the contrary, Mizokami et al. teaches the use of RESYNC detection signals to correct positional sync errors between bifurcated leading and trailing edge data. Thus, there is no showing of how or why one skilled in the would be motivated to change the operation of Mizokami et al., which achieves minimization of frame sync errors by using another methodology. Indeed, the Examiner appears to propose a modification which changes the principle of operation of the reference, whereas such a change is explicitly proscribed by the relevant case law in establishing a *prima facie* case of obviousness under §103(a). *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Additionally, the rejection fails to address the further limitation of "addition bit patterns" before and after the bit pattern having a run length longer that the minimum run length. Thus, a *prima facie* case of obviousness has further not been established since all the claim limitation have not been shown to be met.

With respect to claim 2, the Examiner has further asserted that Mizokami et al. teach the addition bit pattern arranged after the bit pattern has a fixed length referring to column 12, lines 47-64 in support. However, this section of the reference merely teaches that the presence of the pit corresponding to a code train is fixed irrespective of the state immediately before the sync signal. No teaching is given, however, of fixing addition bit patterns in a sync signal. Indeed, neither in this section nor elsewhere in the reference are the claimed limitations of addition bit patterns in the sync signal taught or suggested, not to mention an "addition bit pattern" of fixed length. Thus, the cited reference does not teach or suggest the limitations of claim 2.

Finally, with respect to the rejection of claim 4, the Examiner asserts that Mizokami et al. discloses the claimed limitations except for the sync signal including a specific code indicative of a position in the sector. To make up for this deficiency, the Examiner asserts that Kato et al. discloses a 32 bit cycle redundant check code (CRCC 56 in Figure 2) for indicating a position in a sector and that it would have been obvious to indicate position in a sector using the CRCC as taught by Kato et al. with Mizokami et al. in order to limit the time required to identify frames.

Applicants assert that a *prima facie* case of obviousness has not been established since the references, either taken alone or combined, do not teach or suggest all the limitations of the claimed method. Specifically, claim 4 recites that "said sync signal includes a specific code indicative of a position in said sector." As admitted in the Office Action, Mizokami et al. does not disclose this limitation. Furthermore, Kato et al. also does not teach this specific limitation. It is not clear where or how Kato et al. teaches that the 32 bit CRCC is indicative of a position in a sector. To the contrary, Kato et al. appears to merely teach that the CRCC is used by an error detection and correction circuit for detecting erroneous data and correcting bits by parity (See column 8, lines 57-59). Thus, Kato et al. does not teach the limitations for which it is relied upon.

Further, Kato also does not teach that the 32 bit sync pattern 52 includes a specific code indicative of a position in a sector as required by claim 4. Therefore, in light of the lack of teaching or suggestion of all the claim limitations in the cited references, a *prima facie* case of obviousness has not been established in the rejection of claim 4.

Based on the foregoing remarks, Applicant respectfully submits that this case is in condition for allowance with claims 1-14, and allowance is respectfully solicited.

If any points remain at issue for which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the local exchange number listed below.

Finally, Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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